Claims

[c1] A method of fabricating field effect transistors on a semiconductor substrate comprising

(A) forming rectangular fins of semiconductor material on said substrate in a rectangular pattern of rows and columns, each fin having a top, four sidewalls, a width, a length, and a height H, where the distance between fins in adjacent rows is D; and

(B) irradiating sidewalls of fins in at least one row using radiation at an angle θ to the surface of said sidewall, where $D \approx H \tan \theta$.

[c2] A method according to Claim 1 wherein said substrate is an SOI (semiconductor on insulator).

[c3] A method according to Claim 1 wherein D is about 0.03 to about 0.13 um and θ is about 30 to about 75 degrees.

[c4] A method according to Claim 1 wherein said fins are irradiated at both angle θ and at angle $-\theta$.

[c5] A method according to Claim 3 wherein the top of said fins are implanted with the opposite type of dopant from the sides of the fins.

[c6] A method according to Claim 1 wherein said fins are formed in a square pattern.

[c7] A method according to Claim 1 wherein said fins are formed in a checkerboard pattern.

[c8] A method according to Claim 1 wherein the fins in alternating rows are turned 90 degrees.

[c9] A method according to Claim 1 wherein said fins have a greater length than width and an N-channel transistor and a P-channel transistor are formed on the same fin.

[c10] A fin CMOS transistor made according to the method of Claim 9.

[c11] A method according to Claim 9 wherein said N-channel transistor and said P-channel together form an inverter circuit.

[c12] A method according to Claim 1 wherein said transistors have channels on 2 sides.

[c13] A method according to Claim 1 wherein said transistors have channels on 3 sides.

[c14] A method according to Claim 1 wherein said transistors are surrounded gate transistors.

[c15] A method according to Claim 14 including the step of irradiating sidewalls of fins in at least one column using radiation at an angle θ to the surface of said sidewall, where $D \approx H \tan \theta$.

[c16] A method according to Claim 1 wherein said top and at least 2 of said sides are each separately implanted .

[c17] A method according to Claim 1 wherein sidewalls are coated with a photoresist and a mask is used to form said mask patterns in said sidewalls.

[c18] A method according to Claim 17 wherein said sidewalls are a MEMS (micro electromechanical system).

[c19] A method according to Claim 1 wherein said sidewalls are coated with a photoresist and a mask is used to form contact holes in said sidewalls.

[c20] A method according to Claim 19 wherein said contact holes are electrically connected by a metal layer.

[c21] A method according to Claim 1 wherein the length of said fin exceeds its width and two transistors sharing the same source are fabricated on said fin.

[c22] A fin transistor structure made according to the method of Claim 1 wherein the length of said fin exceeds its width and two transistors sharing the same source are fabricated on said fin.

[c23] A fin transistor according to Claim 22 wherein at least 3 transistors sharing the

same source are fabricated on said fin.

[c24] A method according to Claim 1 wherein, between steps (B) and (C), said fins and substrate are coated with a photoresist, photoresist on said top and one of said sidewalls is exposed using angled radiation and one of said sidewalls and substrate between fins is not exposed, and exposed or unexposed photoresist is removed.

[c25] In a method of fabricating fin-type field effect transistors on a semiconductor substrate, wherein rectangular fins are formed on said substrate, gate electrodes are deposited on at least two sides of said fins, and said gate electrodes are implanted with ions at an angle θ to a line perpendicular to said substrate, the improvement comprising placing said rectangular fins on said substrate in a rectangular pattern of rows and columns such that $D \approx H \tan \theta$, where D is the distance between fins in adjacent rows and H is the height of said fins.

[c26] A method of fabricating field effect transistors on a semiconductor substrate in comprising

(A) forming rows of fins of semiconductor material on said substrate in a rectangular pattern of rows and columns, where each fin has a length sufficient for the fabrication of at least 2 transistors thereon, each fin has a top and four sidewalls, a width, a length, and a height H, where the distance between fins in adjacent rows is D; and

(B) irradiating the sidewalls of fins in one row using radiation at an angle θ to the surface of said sidewall, where $D = H \tan \theta$.